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TOWNSEND and TOWNSEND and CREW LLP

By:_____

PATENT
Attorney Docket No.: 25991A-001200US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Toshiyasu Morita

Application No.: 10/696716

Filed: October 28, 2003

For: PROCESSOR FOR VIRTUAL MACHINES AND METHOD THEREFOR

Customer No.: 20350

Confirmation No. 6473

Examiner: Craig E. Walter

Technology Center/Art Unit: 2188

PROPOSED
PRELIMINARY AMENDMENT

REQUESTED

Ok to enter

/CEW/ 6 April 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to a first Office Action in this application following the Request for Continued Examination, please enter the following amendments and remarks:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. In the listing below, inserted text is marked with underline, deleted text is marked with ~~strikethrough~~, and changes are identified by a vertical bar in the margin.

Listing of Claims:

1-66. (Canceled).

67. (previously presented) A memory access method comprising:

detecting a write operation to a non-volatile memory;

determining an access mode of said non-volatile memory corresponding to a value in a mode register for controlling said non-volatile memory

performing a fast write operation of data to said non-volatile memory in response to a determined access mode that is a first mode;

performing a slow write operation of data to said non-volatile memory, in response to a determined access mode that is a second mode;

responding to a determined access mode that is a third mode by performing a write operation such that:

if an address of said non-volatile memory from a processing logic indicates a write operation to a first address area, then said non-volatile memory write operation is executed according to said fast write operation of data,

if an address of said non-volatile memory does not indicate a write operation to the first address area, then said non-volatile memory write operation is executed according to said slow write operation of data; and

performing a cache write operation of data to a cache memory comprised of a random access memory based on an exception handler routine in response to a determined access mode that is a fourth mode.

68. (previously presented) A memory access method, according to claim 67,

wherein if a cache line of said cache memory contains cache line data other than the data to be written in said cache write operation of said data, said cache line data is written to said non-volatile memory and said data is written to said cache line of said cache memory.

69. (currently amended) A memory access method, according to claim 67, wherein said mode register ~~is indicated~~ indicates an access mode for said non-volatile memory.

70. (previously presented) A memory access method, according to claim 68, wherein said slow write operation has a predetermined write time to said non-volatile memory; and
wherein said fast write operation has a write time shorter than said predetermined time of said slow write time.

71. (previously presented) A memory access method, according to claim 67, wherein said first address area and said second address area is indicated in a register.

72-77. (canceled).

78. (new) A data processing unit comprising:
memory that includes re-programmable non-volatile memory into which data is written; and
control logic that detects a write operation to a non-volatile memory, determines an access mode of said non-volatile memory corresponding to a value in a mode register for controlling said non-volatile memory, performs a fast write operation of data to said non-volatile memory in response to a determined access mode that is a first mode, performs a slow write operation of data to said non-volatile memory, in response to a determined access mode that is a second mode, responds to a determined access mode that is a third mode by performing a write operation such that:

if an address of said non-volatile memory from a processing logic indicates a write operation to a first address area, then said non-volatile memory write operation is executed according to said fast write operation of data,

if an address of said non-volatile memory does not indicate a write operation to the first address area, then said non-volatile memory write operation is executed according to said slow write operation of data, and

performs a cache write operation of data to a cache memory comprised of a random access memory based on an exception handler routine in response to a determined access mode that is a fourth mode.

79. (new) A data processing unit according to claim 78,

wherein if a cache line of said cache memory contains cache line data other than the data to be written in said cache write operation of said data, said cache line data is written to said non-volatile memory and said data is written to said cache line of said cache memory.

80. (new) A data processing unit according to claim 78,

wherein said mode register indicates an access mode for said non-volatile memory.

81. (new) A data processing unit according to claim 79,

wherein said slow write operation has a predetermined write time to said non-volatile memory; and

wherein said fast write operation has a write time shorter than said predetermined time of said slow write time.

82. (new) A data processing unit according to claim 78,

wherein said first address area and said second address area are indicated in a register.

REMARKS/ARGUMENTS

Applicants provide this Proposed Preliminary Amendment, which amends the claims (65-77) pending in this application following the Request for Reconsideration. It is believed the current version of the claims, per this Proposed Preliminary Amendment, will result in claims that are allowable over the art of record.

The previously pending claims include independent claims 65, 73, and 76 that relate to memory with two-speed write operations and independent claim 67 that relates to memory access with four operating modes. The remaining claims are dependent from one or another of these four independent claims. This Preliminary Amendment cancels all previously pending claims relating to the two-speed write operations (claims 65, 66, and 72-77) and retains the claims relating to the four operating modes (claims 67-71). This Preliminary Amendment also adds new claims 78-81 that are directed to a data processing unit with memory having four operating modes. The new claims are apparatus claims that are analogous to the four-mode method claims (67-71). Lastly, claim 69 is amended to correct the wording error that was pointed out in the prior Office Action (dated July 31, 2007), but which was inadvertently uncorrected in the previous amendment filed by Applicants.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 858-350-6100.

Respectfully submitted,

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